LISTING OF THE CLAIMS

1. (Previously Presented) An assembly, comprising:

an integrated circuit die having an array of micro-bumps disposed on a surface of the integrated circuit die in a first pattern;

an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern and an array of solder balls disposed on an outside surface of the integrated circuit package, wherein the first pattern and the second pattern are substantially identical patterns; and

an interposing structure disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package, the interposer coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad located opposite to the first position and to a second landing pad in the array of landing pads.

2. (Previously Presented) The assembly of claim 1, wherein a line extending through the first micro-bump in a direction orthogonal to the surface of the integrated circuit does not extend through the second landing pad of the integrated circuit package.

3. (Original) The assembly of claim 2, wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the interposing structure has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the interposing structure have roughly identical surface areas.

4. (Original) The assembly of claim 3, wherein the interposing structure includes no transistor and no PN junction.

5. (Original) The assembly of claim 4, wherein the interposing structure comprises an array of micro-bumps, wherein the array of micro-bumps of the interposing

structure has a pattern that is substantially identical to the second pattern of the landing pads on the inside surface of the integrated circuit package.

6. (Original) The assembly of claim 5, wherein the interposing structure includes a layer comprising epoxy and fiberglass.

7. (Original) The assembly of claim 5, wherein the interposing structure includes a bypass capacitor.

8. (Original) The assembly of claim 5, wherein the first micro-bump is coupled to the first landing pad at least in part by a conductor disposed in the interposing structure, wherein the conductor disposed in the interposing structure extends in a direction parallel to the surface of the integrated circuit.

Claims 9-11 (Cancelled)

12. (Previously Presented) An assembly, comprising:

an integrated circuit die having an array of micro-bumps disposed on a surface of the integrated circuit die in a first pattern;

an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern and an array of solder balls disposed on an outside surface of the integrated circuit package, wherein the first pattern and the second pattern are substantially identical patterns; and

means for coupling a first micro-bump in a first position in the array of micro-bumps to a first landing pad disposed opposite the first position and to a second landing pad located in a different position in the array of landing pads, the means being disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package.

13. (Original) The assembly of claim 12, wherein the means is also for providing a bypass current to the integrated circuit die.

14. (Original) The assembly of claim 12, wherein the surface of the integrated circuit die is a major surface of the integrated circuit die, and wherein the means has a major surface, and wherein the major surface of the integrated circuit die and the major surface of the means have roughly identical surface areas.

15. (Original) The assembly of claim 12, wherein the means has a planar form and is less than 500 microns thick.

16. (Original) The assembly of claim 12, wherein the integrated circuit die is an application specific integrated circuit (ASIC).